REMARKS

Claims 1-4 are pending in this application, none of which have been amended. No new claims have been added.

The Abstract and specification have been amended to correct minor grammatical, idiomatic and spelling errors. No new matter has been added.

Claims 1-4 stand rejected under 35 USC §103(a) as unpatentable over U.S. Patent 5,428,579 to Robinson et al. (hereinafter "**Robinson et al.**") in view of U.S. Patent 6,332,196 to Kawasaki et al. (hereinafter "**Kawasaki et al.**").

Applicants respectfully traverse this rejection.

Robinson et al. discloses a flash memory card with a power control register that is used to place certain flash memories in a power down mode.

Column 2, lines 6-12 disclose:

> One type of prior flash EPROM used in a prior flash memory card has a standby mode that disables most of the flash EPROM circuitry and reduces device power consumption. The prior flash EPROM also has an active mode. The active mode requires increased power consumption. The active mode is used when the flash EPROM is being written to, read from, or erased.

The Examiner has admitted that **Robinson et al.** does not disclose the buffer memory that data is read into and that when the amount of data stored in the memory falls below a threshold the memory card is then operated in the active mode, as recited in claim 1 of the instant application.

Kawasaki et al. discloses a disk control apparatus comprising a disk controller for

controlling a circuit which controls read operation for reading data from a disk and a CPU for controlling the circuit and the disk controller. The disk controller comprises a buffer memory for storing data for being transferred between a host and the disk controller and a notification section for notifying the CPU that a first state in which an all buffer region of the buffer memory is stored with data to be transferred to the host transmits to a second state in which a predetermined space occurs in the buffer region of the buffer memory as a result of transferring data to the host. The CPU comprises a main control section for stopping power supply to the circuit during the first state and for supplying power to the circuit in response to a notification from the notification section.

Kawasaki et al. teaches only one powered state, which occurs only when a predetermined space occurs in the buffer region by transferring data to the host. The other state in which the buffer is completely full of data to be transferred to the host, consumes no power.

This is in contrast to the present invention, in which there are two power on states, where one is a high (active) mode for reading data from the memory card to the buffer at a high bit rate, and the other is a low (standby) mode in which the memory card waits for a next memory access while the buffer outputs data at a low rate.

Neither of the prior art references teaches, mentions or suggests the relationship between the current consumption and the respective data transfer rates of the card and the buffer, as recited in claim 1 of the instant application.

Thus, the 35 USC §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-4 are in

condition for allowance, which action, at an early date, is requested.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made
Substitute Abstract of the Disclosure

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/745,303

IN THE ABSTRACT:

Amend the Abstract as follows:

A data reproduction device [comprises] including a CPU for reading out data from a memory card having a controller mounted thereon and a DSP for giving the read data required processing. The controller of the memory card is [so] constructed such that an active mode is set for reading out the data under the current consumption of a first current value in response to memory access, and thereafter a standby mode automatically follows for waiting for next memory access under the current consumption of a second current value. The CPU reads out the data intermittently from the memory card at a first bit rate, and store the data to a buffer. The data stored in the buffer is read out at the second bit rate lower than the first bit rate, and supplied to the DSP.

[This contributes to the great reduction of the power consumption.]

IN THE SPECIFICATION:

Amend the specification as follows:

Insert the heading before the paragraph beginning at page 1, line 4 as follows:

BACKGROUND OF THE INVENTION

Delete the heading beginning at page 1, line 10 as follows:

[BACKGROUND OF THE INVENTION]

Paragraph beginning at page 1, line 11 has been amended as follows:

Digital audio players are conventionally known [to] which read compressed audio data on various signal memory media and [to] expand and reproduce the audio data in the memory media. With the players, the data is recorded/reproduced at the bit rate of about 128 K bps, to produce fine quality sound. On the other hand, the development of [the] digital technology in recent years provides various data storage media. Attention is directed to one of the media, IC memory card which is adapted to write and read data at [the] a high bit rate[,] of about a maximum of 8 Mbps.

Paragraph beginning at page 1, line 21 has been amended as follows:

Digital audio players having an IC memory card for use as a data storage medium [are] have been developed. In the digital audio players, data is written/read to an IC memory card at the bit rate of about 128 Kbps in conformity with the bit rate for decoding which is satisfactory [in] with respect [of] to sound quality. The power consumption of the IC memory card is generally constant during memory access regardless of the difference in the bit rate for data writing/reading.

Paragraph beginning at page 2, line 5 has been amended as follows:

With the digital audio player having the IC memory card for use as the data storage medium, the use of a primary or a secondary battery as power source can realize its portability. However, the audio player of the portable type has [the] a problem in that the player is endurable to be used within the limited period of time [since] because the primary or [the] secondary battery is limited in capacity.

Paragraph beginning at page 2, lie 13 has been amended as follows:

An object of the present invention is to provide a data reproduction device such as a digital audio player, etc., which has a memory card, and to prolong the period of time during which the player is endurable to be used by reducing its power consumption.

Paragraph beginning at page 2, line 24 has been amended as follows:

The controller of the memory card is [so] constructed such that an active mode is set wherein data is read out under current consumption [in] at a first current value in response to memory access of data reading, and thereafter a standby mode automatically follows to wait for next memory access under current consumption [in] at a second current value which is lower than in the first current value.

Paragraph beginning at page 3, line 14 has been amended as follows:

With the data reproduction device of the present invention, when a user manipulates to reproduce data, the control circuit repeats the operation to access [to] the memory card, and to

read out intermittently predetermined amount of data from the memory card at the first bit rate. The read data is stored in the buffer.

Paragraph beginning at page 4, line 23 has been amended as follows:

With the data reproduction device of the present invention, as described, [since] because power consumed by the memory card for reading out all the data to be reproduced is a total value of the power consumption in both the active mode and [that in] the standby mode, the power consumption is [more] reduced more than in the conventional case where the memory card is always accessed at the low bit rate which does not have a problem in data reproduction, to continue great current consumption.

Paragraph beginning at page 5, line 15 has been amended as follows:

A digital audio player embodying the present invention will be described below in detail with reference to the drawings. FIG. 1 shows that the digital audio player of the present invention can be loaded with a memory card 8 having a controller 9 mounted thereon. The audio player comprises a memory card controller 7 to control write/read of data to the memory card 8, a CPU 1 to execute various controlling operation like data reproducing in response to user's manipulation, a digital signal processing circuit DSP 3 to perform processing required for reproduction [like] such as decoding, etc., on audio data read out from the memory card 8, a D/A converter 4 to convert digital audio signal obtained from the DSP 3 into analog audio signal, an amplifier 5 to amplify the audio signal obtained from the D/A converter 4 and to output the

signal to a headphone 6. The CPU 1 has a buffer 2 incorporated therein, and is connected to a manipulating key 10 for a user giving the device a command for various operation.

Paragraph beginning at page 6, line 9 has been amended as follows:

The controller 9 mounted on the memory card 8, as shown in FIG. 3, sets an active mode A to read out data under [the] a current consumption of 33 mA in response to memory access of data reading. If there is no memory access within a predetermined period of time T, a standby mode S automatically follows to wait for the next memory access [under] at [the] a current consumption of 50 μA.

Paragraph beginning at page 6, line 20 has been amended as follows:

FIG. 2 shows a controlling procedure which the CPU 1 executes in data reproduction. An inquiry is made in step S1 as to whether the PLAY key is turned on by a user's manipulation. When the PLAY key is on, the CPU 1 commands the memory card controller 7 to read the data from the memory card 8 in step S2. This sets the memory card 8 in the active mode, to read the predetermined amount of data from the memory card 8 at the bit rate of 8 Mbps. When reading data access (active mode) from the memory card ends and the predetermined period of time T (=5 ms) elapses, the memory card 8 [is] goes into the standby mode.

Paragraph beginning at page 9, line 5 has been amended as follows:

If data is successively read out from a memory card at the conventional bit rate of 128

Kbps [as conventionally] in place of the intermittent reading method of the memory card according to the embodiment, the consumed current is a constant 33 mA [in constant], so that the power consumption is minimized to 1/17 or less according to the present invention. The increase of the capacity of the buffer 2 of the CPU 1 provides greater effect.

Paragraph beginning at page 9, line 13 has been amended as follows:

The present invention described is particularly effective [to the] for a portable data reproduction device [of the portable type since] because the intermittent data read out from the memory card enables the device to reduce the power consumption greatly.